Double-Layer No-Flow Underfill Materials and Process

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***Abstract*—The no-flow underfill has been invented and practiced in the industry for a few years. However, due to the interfering of silica fillers with solder joint formation, most no-flow underfills are not filled with silica fillers and hence have a high coefficient of thermal expansion (CTE), which is undesirable for high reliability. In a novel invention, a double-layer no-flow underfill is implemented to the flip-chip process and allows fillers to be incorporated into the no-flow underfill. The effects of bottom layer underfill thickness, bottom layer underfill viscosity, and reflow profile on the solder wetting properties are investigated in a design of experiment (DOE) using quartz chips. It is found that the thickness and viscosity of the bottom layer underfill are essential to the wetting of the solder bumps. Chip scale package (CSP) components are assembled using the double-layer no-flow underfill process. Silica fillers of different sizes and weight percentages are incorporated into the upper layer underfill. With a high viscosity bottom layer underfill, up to 40 wt% fillers can be added into the upper layer underfill and do not interfere with solder joint formation.**

***Index Terms*—Assembly yield, design of experiment, flip-chip, no-flow underfill, silica fillers.**

I. Introduction

THE flip-chip technology has drawn tremendous attention in electronic packaging over the last 20 years due to its advantages over other first level interconnection methods including high input/output (I/O) counts, better electrical performance, high throughput, and low profile, etc. [1]. The market demands for smaller, lighter and faster electronic products with higher performance, more functionalities and, yet, even lower cost, have resulted in the increasing use of organic substrates instead of ceramics. In order to alleviate the thermal stress on the solder joint caused by the difference between the coefficient of thermal expansions (CTE) of the silicon and the organic substrate, underfill was invented and its application in flip-chip has greatly enhanced the package reliability [2], [3]. However, the current underfill process encounters various problems. The conventional underfill is drawn into the gap between the chip and the substrate by the capillary flow, which is usually slow and can be incomplete, resulting in voids. It also produces nonhomogeneity in the resin/filler system. In addition, curing of the underfill takes hours in the oven [4]. As the gap distance gets smaller, flux cleaning becomes difficult. The incompatibility of the underfill and flux residual creates interfacial adhesion problems in the package and lowers the reliability. These problems aggravate further with the increase in chip dimensions and I/O counts, and the decrease in gap distances and pitch sizes.

In order to address the problems associated with conventional underfill, several innovative approaches have been developed, including no-flow underfill, molded underfill and wafer level underfill. In the no-flow underfill process, the underfill is dispensed onto the substrate prior to the chip placement. The underfill usually has the fluxing capability to facilitate the solder to wet on the contact pads of the substrate during the solder reflow. This technology simplifies the underfill process by eliminating the capillary flow and combining the solder reflow and underfill curing into one step [5]. It has been developed for several years and evaluated in industries. However, due to the interference of silica fillers with solder joint yield [6], no-flow underfills are mostly unfilled or of very low filler loading. The high CTE of the material limits the package reliability, especially in the case of large dies. Since epoxy molding compounds (EMCs) have been used in component packaging for a long time, by adjusting the silica fillers and modifying the board design, epoxy molding compound (EMC) can be molded to fill the gap under the chip [7], [8] and applied as the over-mold as well. However, the material and process still need to be optimized, and molded underfill is limited to the flip-chip in package. By applying the underfill onto the wafer, wafer level underfill process suggests a convergence of front-end and back-end in package manufacturing and may enable low cost, high reliability flip-chip assembly for high-end applications [9]. However, wafer level process presents great challenges to underfill materials. Not only do they have to be compatible with the single reflow process similar to no-flow underfill, but also be subjected to wafer process such as coating and dicing [10].

In a novel patented process, a double-layer no-flow underfill is used to incorporate silica fillers into no-flow underfill [11], [12]. Since the previous study has shown that in the filled no-flow underfill, the main cause of low yield in assembly is the entrapment of silica fillers between the solder bumps on the chip and the contact pads on the board, it is realized that if the fillers can be prevented from entering into the gap between the solder bumps and contact pads, they will not interfere with the formation of the solder joint. In this patented process, two layers of no-flow underfill are applied. The bottom layer underfill is relatively high in viscosity and is not filled with silica fillers. It is applied onto the substrate first; then the upper layer underfill which is filled with silica fillers is dispensed. The chip is then placed onto the substrate and reflowed, during which the solder joints are formed and the underfill is cured or partially cured. The process flow chart is illustrated in Fig. 1.

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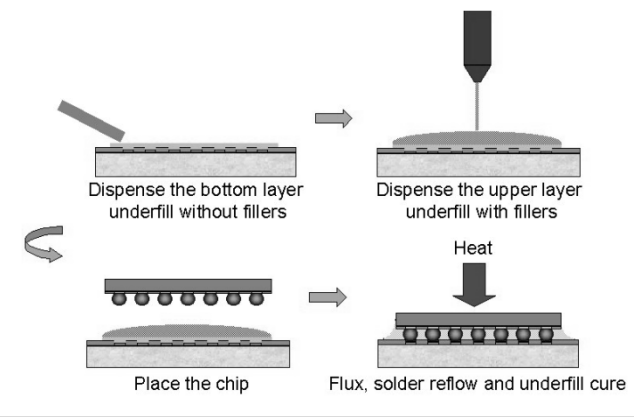

Fig. 1. Double-layer no-flow underfill process.

In this paper, the fundamental aspects for processability of the double layer no-flow underfill are studied. The important materials and process parameters affecting the yield of flip-chip interconnection with filled no-flow underfill are investigated.

II. Experimental

A. Materials

The no-flow underfills used in this study were all in-house developed. Three types of bottom layer underfill were investigated. They are named as BLV, BMV, and BHV, indicating the viscosity is low, medium, and high, respectively. The upper layer underfill was filled with different sizes and different loadings of silica fillers. It is named as UXX-YY with the first two digitals XX indicating the average particle size (μm) of the silica filler and the last two digitals YY indicating the weight percentage (YY wt%)of silica fillers. For instance, U07-40 is an upper layer underfill with 40 wt% filler loading and the average filler size is 7 μm. U0 is the base formulation of the upper layer underfill without silica filler.

B. Characterization

The viscosities of the three bottom layer underfills were measured using a stress rheometer (AR 1000 N by TA Instruments) under oscillation mode. A cone-and-plate geometry was used and the experiments were conducted at a frequency of 10 Hz and an oscillation stress of 500 Pa. The heating rate used in the experiments was 20 °C/min from 20 °C to 160 °C.

The curing behavior of the three bottom layer underfills was characterized using a modulated differential scanning calorimeter (DSC Model 2920, by TA Instruments). A sample of about 10 mg was placed into a hermetic DSC sample pan and put in the DSC cell under 40 ml/min Nitrogen purge. The heat flow during curing at a heating rate 5 °C/min was recorded for each underfill formulation.

C. Assembly

The material and process parameters investigated in this paper include:

- thickness of the bottom layer underfill;
- viscosity of the bottom layer underfill;
- reflow profile;
- filler loading of the upper layer underfill;
- filler size of the upper layer underfill.

TABLE I
Details of the Experimental Design

	Reflow Profile	Bottom Layer	Thickness
#1	Standard	BLV	35μm
#2	Standard	BLV	70μm
#3	Standard	BMV	35μm
#4	Standard	BMV	70μm
#5	Modified	BLV	35μm
#6	Modified	BLV	70μm
#7	Modified	BMV	35μm
#8	Modified	BMV	70μm

Since these parameters might interact with each other in determining the yield of the double-layer no-flow underfill process, the preliminary experiments were carried out using eutectic Sn/Pb bumped quartz chips and Ni/Au coated Cu substrates as test vehicles in a design of experiment (DOE). The bumps were area-array distributed; the height and diameter of the bumps was 75 μm and 75 μm, respectively. The independent variables investigated were the thickness and the viscosity of the bottom layer underfill and the reflow profiles.

The details of the experimental design are listed in Table I. To control the thickness of the bottom layer underfill, two types of Kapton® tape (from Shercon) were used as spacers. The tapes were laminated onto the substrate, which was heated up to 90 °C. The bottom layer underfills were applied onto the heated substrate and a glass slide was used as a blade to even the underfill surface. Then the substrate was cooled down to the room temperature and the tapes were removed. Measured by a laser profilometer, the average thickness of the bottom layer underfill was about 35 μm when the thinner tape was used and 70 μm when the thicker tape was used. Two types of bottom layer underfill were evaluated, BLV with low viscosity and BMV with medium viscosity. The upper layer underfill used in this DOE was U07-60. After the dispensing of the upper underfill layer, the quartz chip was flipped and placed onto the substrate and was subjected to the reflow process in a BTU seven-zone reflow oven. The two reflow profiles (standard and modified) are shown in Table II.

To further evaluate the double-layer no-flow underfill process, CSP components with daisy-chained bumps were used in the assembly. There are 98 bumps per component and they are daisy-chained into three channels in addition to two separate testing points. The electrical continuity of each channel together with the two separate testing points can be tested. The diameter of the bumps on the CSP components is 300 μm with a pitch size of 500 μm. There are eight sites on each substrate. The contact pads are solder mask defined and the surface finish of the contact pads is Cu/OSP. The solder mask thickness is around 40 μm. A picture of the assembled substrate is shown in Fig. 2. The bottom layer underfill was dispensed in the same way described in the previous text. A K&S Assembly System was used to place the components onto the board. Before solder reflow, the alignment was examined using an X-ray inspection machine (NIS, NXR-1525).

TABLE II
TEMPERATURES OF 7-ZONE REFLOW PROFILES USED IN DOE

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7
Standard (°C)	100	150	150	150	180	230	230
Modified (°C)	100	150	150	180	230	200	180

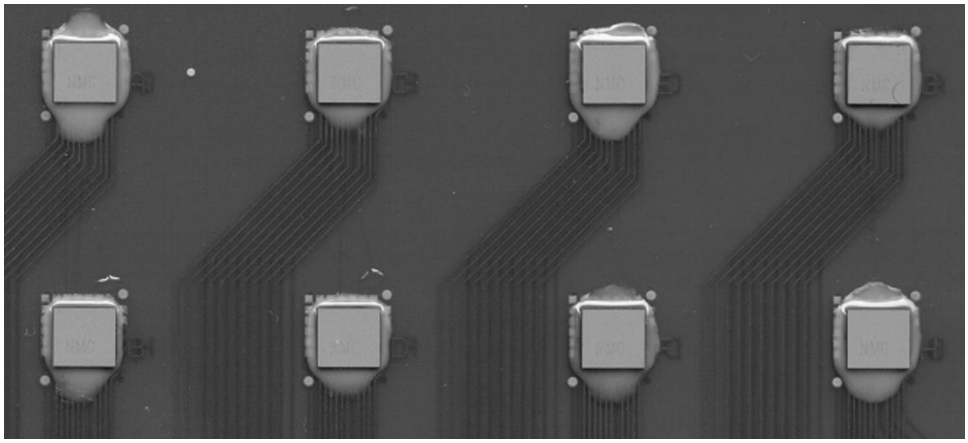

Fig. 2. Picture of the assembled substrate.

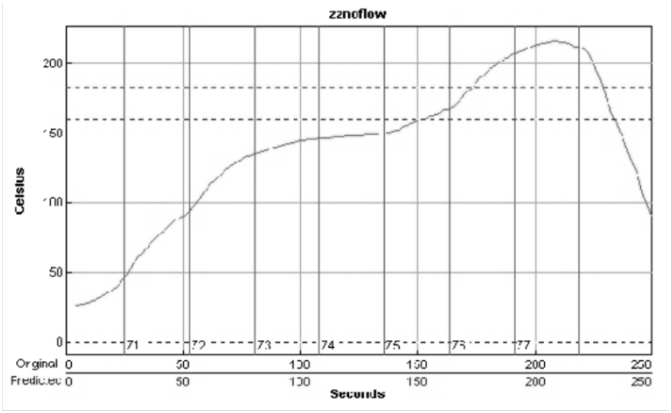

Fig. 3. Temperature profile in the standard reflow process.

The parameters investigated in this experimental design were the viscosity of the bottom layer underfill, the size of the fillers in the upper layer underfill and the filler loading in the upper layer underfill. Only standard reflow profile was used. The temperature profile of the reflow process was measured using thermocouples placed on the substrate and was shown in Fig. 3. The two upper layer underfills used in the assembly of the CSP components were BMV and BHV with a thickness of 35 μm. The details of underfills used in the assembly are listed in Table III.

TABLE III
UNDERFILLS USED IN THE ASSEMBLY OF CSP COMPONENTS

Sample No.	Bottom Layer	Upper Layer
01	BMV	U0
02	BHV	U0
1	BMV	U07-20
2	BMV	U07-40
3	BMV	U07-60
4	BHV	U07-20
5	BHV	U07-40
6	BHV	U07-60
7	BMV	U15-20
8	BMV	U15-40
9	BMV	U15-60
10	BHV	U15-20
11	BHV	U15-40
12	BHV	U15-60

III. RESULTS AND DISCUSSION

A. Material Characterization

One important material property of the no-flow underfill relating to the process yield is its change of viscosity with respect to temperature. For a normal no-flow underfill, a high curing latency is required so that the underfill can maintain a low viscosity at the solder reflow temperature. Otherwise, the gelled underfill will hinder the solder wetting on the contact pads and forming interconnection. However, in the double-layer no-flow underfill process, high viscosity of the bottom layer underfill is required to prevent the filler from settling onto the pad and interfering with solder joint formation. Fig. 4 shows the magnitude of the complex viscosity of the three bottom layer underfills and one upper layer underfill U07–40 with respect to the change in temperature. It can be seen that at all temperature ranges, the three bottom layer underfills possess higher viscosity than the upper layer underfill. Fig. 5 shows the complex viscosity and the delta degree of the three bottom layer underfills. With increasing temperature, the viscosity of the underfill decreases quickly, and the material undergoes a transition from an elastic solid to a viscous fluid. In the transition region, it shows viscoelastic behaviors. Since the bottom layer underfill is solid-like during room temperature, fillers cannot enter the gap between the solder bump and the contact pad. At a higher temperature, with the decrease in viscosity, the underfill becomes fluid-like, and the solder bump might be able to penetrate this layer and

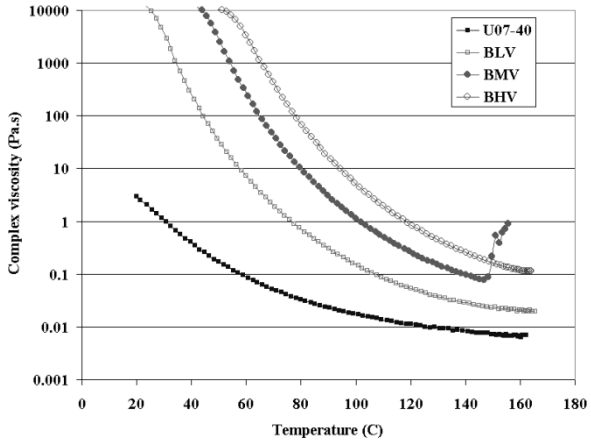

Fig. 4. Complex viscosity of the bottom layer underfills and one upper layer underfill.

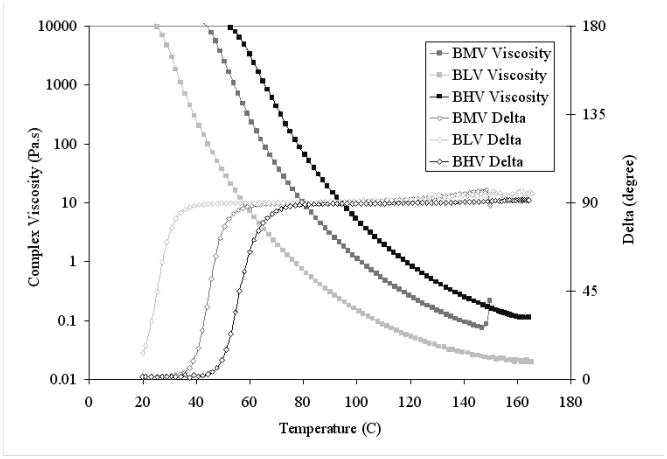

Fig. 5. Complex viscosity and delta degree of the bottom layer underfills.

make contact with the contact pad. So the change of the viscosity with respect to temperature is crucial to this process. The curing behavior of the three bottom layer underfills was illustrated in Fig. 6. As can be seen in the figure, the curing behaviors of these three formulations are very similar to each other. All of them have enough curing latency and fluxing capability to allow solder to melt and wet on the contact pad before gelation takes place.

B. Effects of the Underfill Viscosity, Thickness and Reflow Profile on Solder Wetting

The effects of the viscosity and thickness of the bottom layer underfill and the solder reflow profile on the solder wetting were investigated in the assembly of quartz chips and observed using an optical microscope and shown in Fig. 7. The observation of quartz chip wetting behavior suggested that the viscosity and the layer thickness of the bottom underfill are important to this process while the reflow profile does not have a significant effect on the wetting. When the medium viscosity bottom layer was applied, thinner layer showed better wetting; when the low viscosity bottom layer was applied, thicker one showed better wetting.

The results indicated that solder wetting is complicated in this double-layer no-flow underfill process. Since the solder reflow is a dynamic process, the wetting of solder on the pad will be determined by several simultaneous procedures including the decrease in underfill viscosity, the collapsing of the chip, the settling of the fillers, the curing of underfill, and the solder melting. In the case of the low viscosity bottom layer underfill, the transition from a solid-like material to a fluid-like material occurs at low temperature and hence, early in the process as indicated by the viscosity results in Fig. 5. As such, with a thinner layer, the fillers can easily settle down onto the Cu board, which leads to poor solder wetting. In the case of the medium viscosity bottom layer underfill, the material remains solid-like at elevated temperature, and thus prevents the filler settling. But if this layer is too thick, it will prevent the chip from collapsing onto the Cu board, causing poor solder wetting.

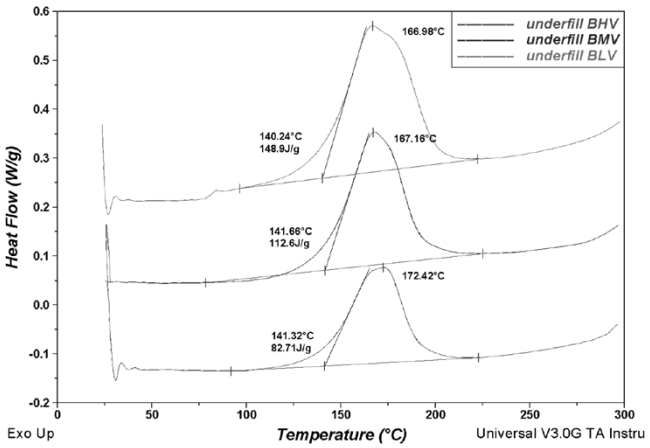

Fig. 6. DSC curing behavior of the bottom layer underfills.

It was also observed in the assembly of quartz chip that the chip usually moved after the reflow when low viscosity bottom layer underfill was used. This chip movement was confirmed in the assembly of CSP components. Figs. 8 and 9 show the X-ray image of the component after the placement by the K&S Assembly System and after solder reflow process. Since the pitch size of CSP components is large, there is no difficulty in the alignment of the components to the board. However, 7 out of 8 components assembled with low viscosity bottom layer underfill (BLU) showed misalignment after reflow. This happened disregarding the thickness of the bottom layer while it did not occur to any of the components assembled with medium and high viscosity bottom layer underfills (BMV and BHV). One possible reason is that the flow of the underfill due to the change in viscosity might have moved the components on top and hence caused the misalignment. As observed in Fig. 5, the BLV has its solid-to-fluid transition at room temperature and it might have enough fluidity to cause significant component movement before the solder reflow. Although the higher viscosity ones (BMV and BHV) also have the similar transition, it happens at relatively higher temperature and the flow of the underfill might not be significant enough to move the component above totally off the pad before the solder starts to melt and wet the contact pad, from which the solder self-alignment takes place. However, this might become a possible concern for flip-chip application where the pitch size is much smaller.

C. Effects of Filler Size and Loading on the Solder Joint Yield

According to the results from the preliminary experiments, bottom layer underfill with high viscosity and thin thickness is

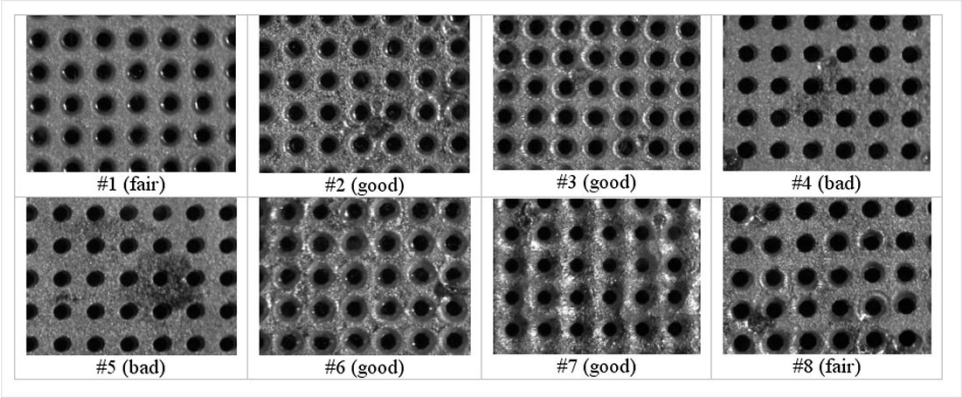

Fig. 7. Pictures of quartz chips after reflow.

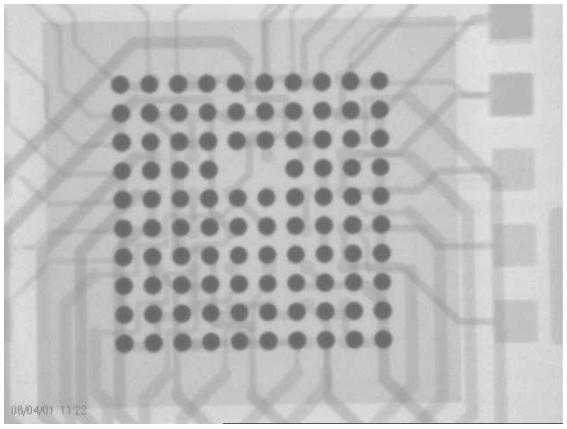

Fig. 8. X-ray image of the assembly after placement.

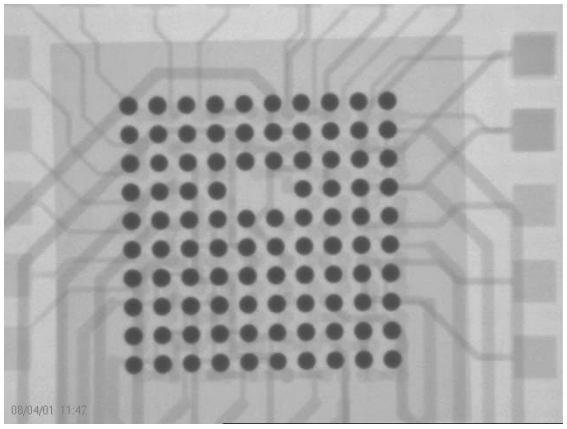

Fig. 9. X-ray image of the assembly after reflow with low viscosity.

preferred in the assembly of the double-layer underfill, since thin bottom layer underfill increases the overall filler concentration given the same filler loading in the upper layer underfill. Hence, in the assembly of CSP components, underfills BMV and BHV were applied with a thickness of 35 μm. Only the standard reflow profile was used, since it was found that the reflow profile did not show a significant effect on the solder wetting.

The electrical continuity of each component after reflow is listed in Table IV. All three channels together with the two separate testing points were tested. The results from the table obviously favored HV over MV in the bottom layer underfill. For filler content, up to 40 wt%, the yield was reasonable. The results favored the smaller filler size over the larger one.

TABLE IV
ELECTRICAL CONTINUITY OF THE CSP COMPONENTS AFTER REFLOW

No.	R1	R2	R3	S1	S2
01	√	√	√	√	√
02	√	√	√	√	√
1	×	×	×	√	×
2	×	×	×	×	×
3	×	×	×	×	×
4	√	√	√	√	√
5	√	√	√	√	√
6	×	×	×	√	√
7	×	√	√	√	√
8	×	×	×	×	×
9	×	×	×	×	×
10	√	×	√	√	√
11	×	√	√	√	√
12	×	√	×	×	×

Note: Check indicates pass; x indicates failure

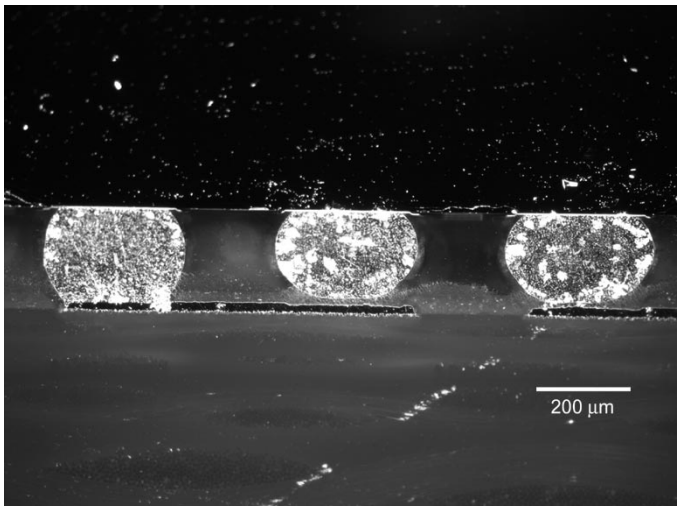

Fig. 10. Cross section view of component #1.

In order to further exam the solder joint formation, all the samples were cross-sectioned and observed under the Leica DML 300 optical microscope. Figs. 10–15 are pictures of cross sections of a few components. Figs. 10 and 11 show the cross section views of component #1, in which the medium viscosity

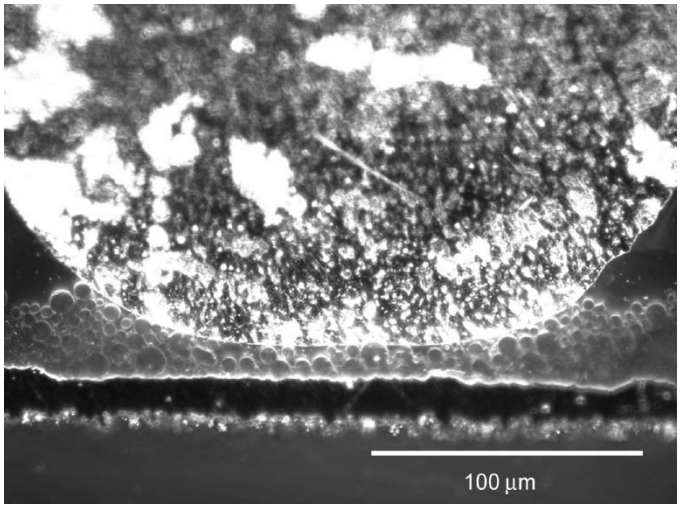

Fig. 11. Filler settling and trapped in component #1.

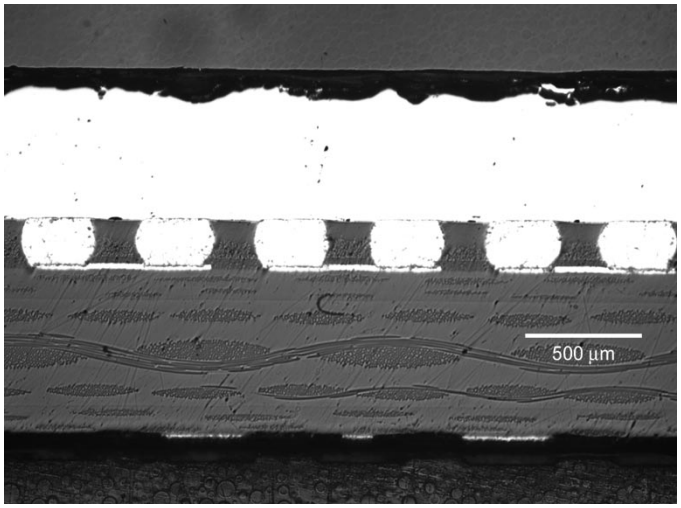

Fig. 12. Cross section view of component #5.

bottom layer underfill (BMV) was used and filler loading was 20 wt%. Even if the filler concentration was not high, the overall yield was very low as shown in Fig. 10. Fig. 11 clearly indicates the settling of the silica filler when the viscosity of the bottom layer underfill is not high enough.

When the high viscosity bottom layer underfill (BHV) was used, the situation was much better. Figs. 12 and 13 illustrate the cross section of component #5, in which 40 wt% of silica filler was added. Although the filler settling was still obvious as can be seen in Fig. 13, the high viscosity bottom layer was able to exclude the fillers from the solder joint. However, if the filler content was further increased, there were occasionally fillers trapped in between the solder bumps and contact pads as shown in Fig. 14, although the filler distribution across the underfill seemed more uniform.

In the previous cross sections shown, silica fillers with average size of 7 μm were used. Fig. 15 shows the cross section view of component #11, in which BHV was used as the bottom layer underfill and silica fillers with average size of 15 μm were used at 40 wt%. As can be seen in the picture, larger fillers had a higher tendency to settle down, causing the failure of solder joint formation.

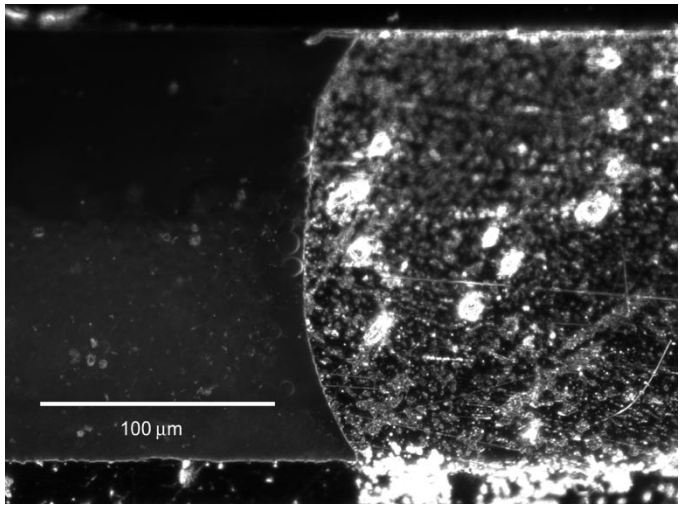

Fig. 13. Solder joint integrity in component #5.

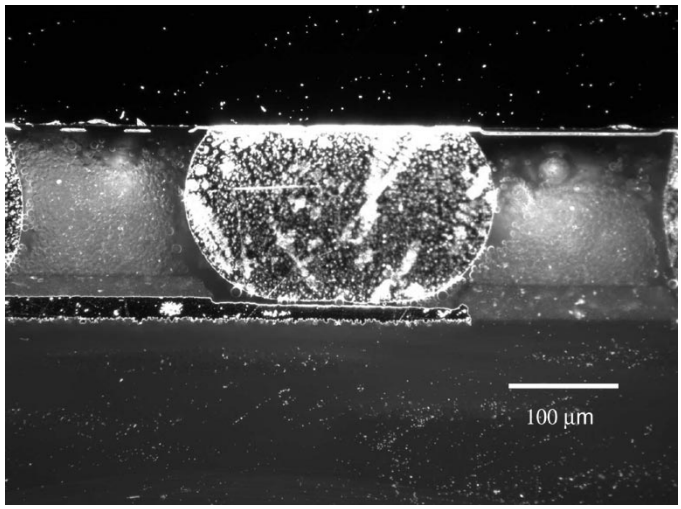

Fig. 14. Failed solder joint in component #6.

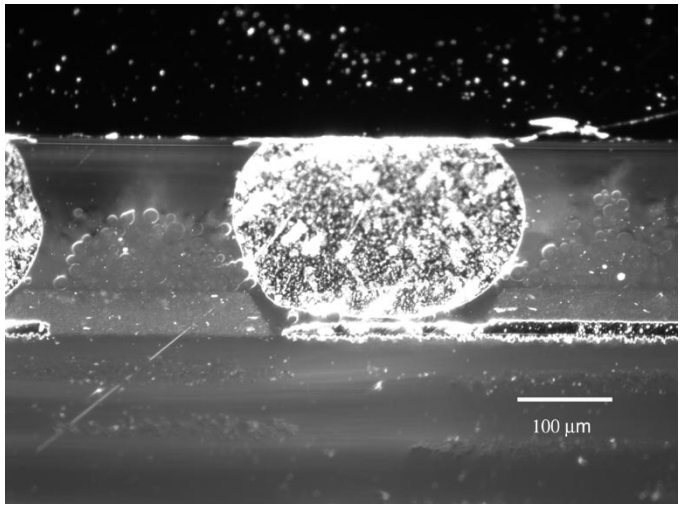

Fig. 15. Failed solder joint in component #11.

The results from the assembly of the CSP components suggested a narrow process window for the double-layer no-flow underfill. However, all the factors affecting the solder joint yield are interacting with each other. For instance, if the viscosity of the bottom layer underfill is increased further and the solid-to-fluid

transition can be pushed to a higher temperature, it can prevent the filler settling more effectively and higher filler loading can be used. On the other hand, if we can adjust the filler size and loading to minimize the filler settling, the yield can be increased using a bottom layer underfill of relatively low viscosity. Furthermore, the experimental consistancy is another issue. In these experiments, all the bottom layer underfills were manually dispensed onto the board when the temperature of the board was elevated. The films that formed on the board were not defect-free and the thickness varied at different locations. If the dispensing process is better controlled and uniformity of the bottom layer underfill can be achieved, the solder joint yield can be enhanced further.

The process of the double-layer no-flow underfill is also closely related to the chip and board design. It was observed that using the same material and process parameters, quartz chip and CSP component can show different yields. The diameter of the solder bump, the pitch size, and the pad design on the board can be important parameters affecting the yield. Further work is needed in order to implement the double-layer no-flow underfill process to the flip-chip assembly. Nevertheless, it offers a potential option in enhancing the solder joint reliability by incorporating fillers into no-flow underfill.

IV. Conclusion

The double-layer no-flow underfill process is a novel process that allows silica fillers to be incorporated into the no-flow underfill and hence reduces the CTE of the underfill and enhances the reliability of flip-chip packages. However, factors affecting the interconnection yield of the double-layer no-flow underfill are complicated and interacting with each other. According to the results from the assembly of quartz chips, the thickness and the viscosity of the bottom layer underfills are essential to the wetting of the solder bumps. CSP components were successfully assembled using the double-layer no-flow underfill process. Upper layer underfills with different filler sizes and loadings were used in the assembly. With high viscosity bottom layer underfill, up to 40 wt% fillers can be added into the upper layer underfill and do not interfere with solder joint formation. Filler settling is a concern when larger size fillers are used. At high filler loading, the settled fillers can be trapped in between the solder bumps and contact pads and cause failure in interconnection.

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